



Automated Problem and Solution Generation Software for Computer-Aided Instruction in Elementary Linear Circuit Analysis

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Motivation

- Linear circuit analysis is a foundational topic in electrical engineering, and is frequently also required of nonmajors, for whom it may be most or all of their exposure to electrical engineering

- Students frequently struggle with such courses for several reasons, in our opinion:
 - Misconceptions about electricity coming into course, which may be frequently unrecognized by instructors¹
 - Insufficient interactive activities
 - Delayed feedback on homework and assessments
 - Lack of sufficient worked examples to lead students gradually up to the level of homework problems

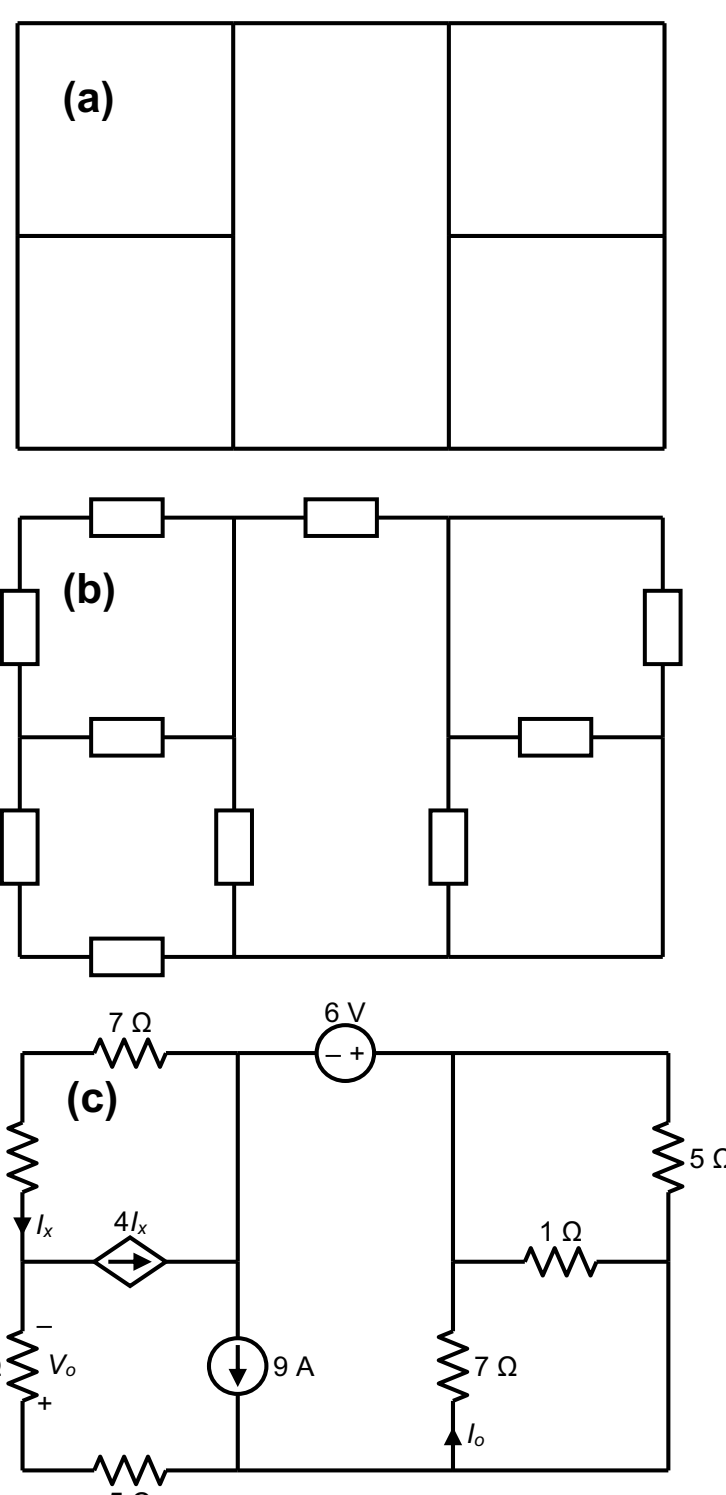
- This project aims to develop and rigorously assess novel cyberlearning tools to improve student mastery of this subject through practice in a highly interactive system capable of providing immediate, accurate, and highly relevant feedback regarding errors to both the students and their instructors

- Special problem types to focus on qualitative understanding and typical student misconceptions will be included

- Software can be used in many ways, to generate automatically gradable homework sets and exams, interactive exercises for use during class, textbook problems & examples, and in a full tutorial system designed to supplement conventional instruction

- Tutorial system is being developed to use these tools, adapting to individual student needs and providing real-time feedback to instructors regarding student difficulties

Three-step Process for Circuit Generation



Circuit Generation Procedure

- Circuits are generated as layouts, not netlists, since beginning students may not recognize the equivalence of circuits laid out differently, and specifying layouts guarantees planar circuits suitable for mesh analysis

- All circuits are laid out on a square grid of points for convenience; any planar circuit can be represented this way

- Randomly placing circuit elements on a grid and then checking them for validity is not a workable approach for anything other than very small circuits; the number of possibilities is vast and only a tiny fraction are valid

- We therefore use a three-step process for circuit generation, using special algorithms at each stage designed to maximize the probability of circuits being valid

- First step involves placing "shorts" and "opens" on the square grid; opens always stay open, but some of the shorts are later changed to circuit elements [Fig. 1(a)].

- Second step changes the required number of shorts into generic circuit elements, which are later changed to specific elements [Fig. 1(b)]

- Third & final step changes the generic elements into specific circuit elements, assigns values and polarities, control variables for dependent sources, and gains [Fig. 1(c)]¹⁰

Typical Student Misconceptions¹

- "Sequential" reasoning: Circuit elements only affect those that "follow" them in a loop around the circuit

- Batteries as current sources: Connecting a second light bulb in parallel with one in parallel with a battery causes the first one to dim by siphoning off part of its current

- Current or charge is "used up" in a resistor

- Open circuits must have zero voltage across the gap

- Inappropriate applications of Ohm's law (e.g., to voltage sources, or to voltages & currents that do not appear across same resistor)

- Applying superposition to powers

- Term confusion of current, voltage, and power (e.g., voltage and current must always exist together)

- Resistance exists only when current is flowing

- Local reasoning: Current divides equally at every junction, regardless of the rest of the circuit

- Battery superposition: More batteries provide more power to a circuit, regardless of their connection

- Incorrect identification of series & parallel connections

- Thinking that voltage sources have no current through them, and/or that current sources have no voltages across them

Pedagogical Feature: Relating Terms in KCL Equation to Currents Leaving a Supernode

Problem #1

Circuit Diagram with Node Analysis

Compute the following 2 quantities for this circuit:

V_1 , I_4

Each colored arrow corresponds to a term in KCL equation #3 of 3.

Voltage constraint equations:

$V_1 = 3V_2$

$V_2 - V_3 = 5V$

KCL equations for each node or supernode:

$\frac{V_1}{6\Omega} + \frac{V_2 - V_1}{7\Omega} + \frac{V_2 - V_3}{1\Omega} + \frac{V_2 - V_3}{3\Omega} = 0$

$-5A + \frac{V_2 - V_3}{3\Omega} + \frac{V_3 - V_2}{3\Omega} = 0$

$\frac{V_1 - V_2}{9\Omega} + \frac{V_2 - V_3}{1\Omega} + \frac{V_3 - V_2}{3\Omega} = 0$

Equations for control variables of dependent sources:

$V_2 = V_1 - V_3$

Matrix form of node equations:

Circuit Specs | Display Options | Element Values | Sought Values | Solution Display

Element Labeling

Values (e.g., 5 V)

Names (e.g., V2)

Color nodes

Node/Mesh Labeling

Score (Series/Parallel)

Start Series/Parallel

Completed w/ no errors: 0

Correct % = 0

Indices of Series/Parallel Groups to Highlight Red

Series Group

Parallel Group

None

None

None

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Pedagogical Feature: Relating Terms in KVL Equation to Voltage Drops Around a Supermesh

Problem #1

Circuit Diagram with Mesh Analysis

Compute the following quantity for this circuit:

V_2

Each colored +/- symbol pair corresponds to a term in KVL equation #2 of 3.

Current constraint equations:

$I_1 - I_2 = 5A$

KVL equations for each mesh or supermesh:

$(1) -4V + (I_1 - I_2)(8\Omega) - 3V = 0$

$(2) -I_2(8\Omega) + 4V - 1V - I_2(8\Omega) - I_2(8\Omega) = 0$

$(3) -I_2(8\Omega) + 5V(3) + 5I_2(3) + I_2(8\Omega) + I_2(8\Omega) = 0$

Equations for control variables of dependent sources:

$I_1 = I_2$

Matrix form of mesh equations:

Circuit Specs | Display Options | Element Values | Sought Values | Solution Display

Element Labeling

Values (e.g., 5 V)

Names (e.g., V2)

Color nodes

Node/Mesh Labeling

Score (Series/Parallel)

Start Series/Parallel

Completed w/ no errors: 0

Correct % = 0

Indices of Series/Parallel Groups to Highlight Red

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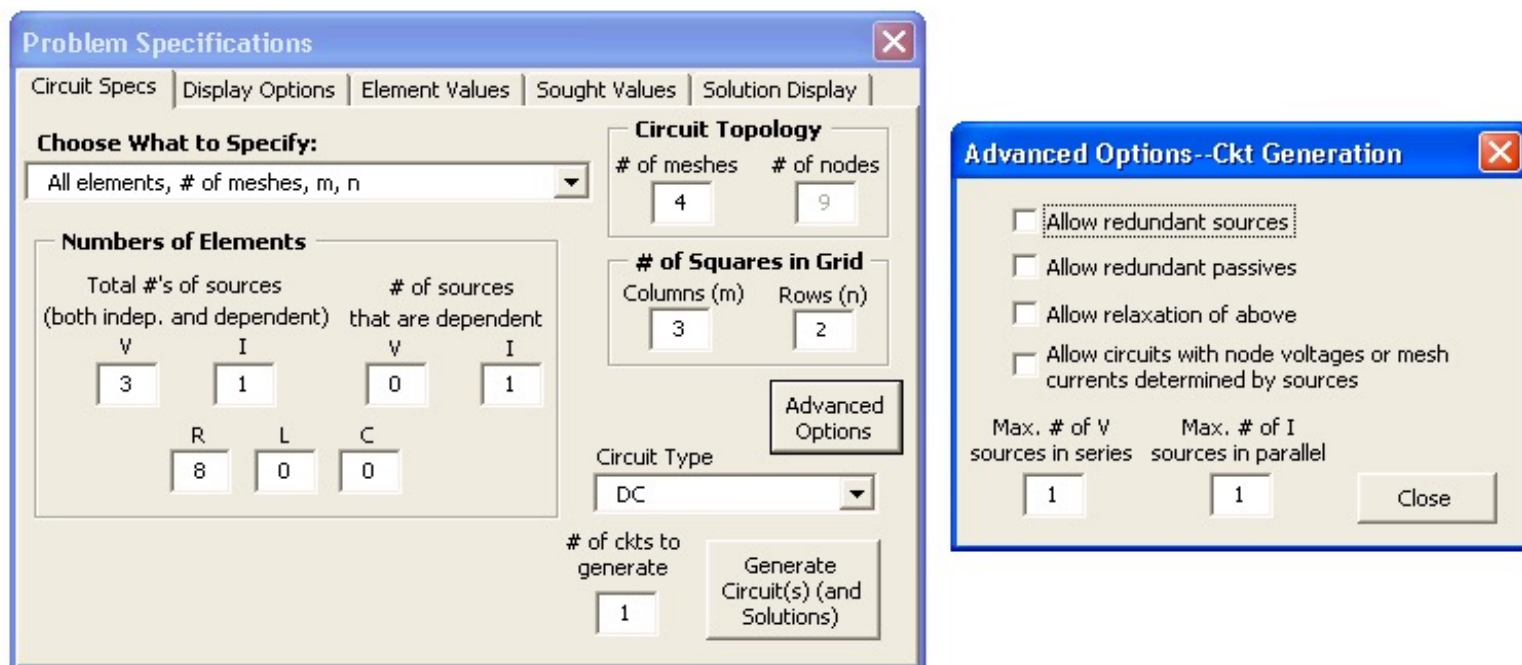
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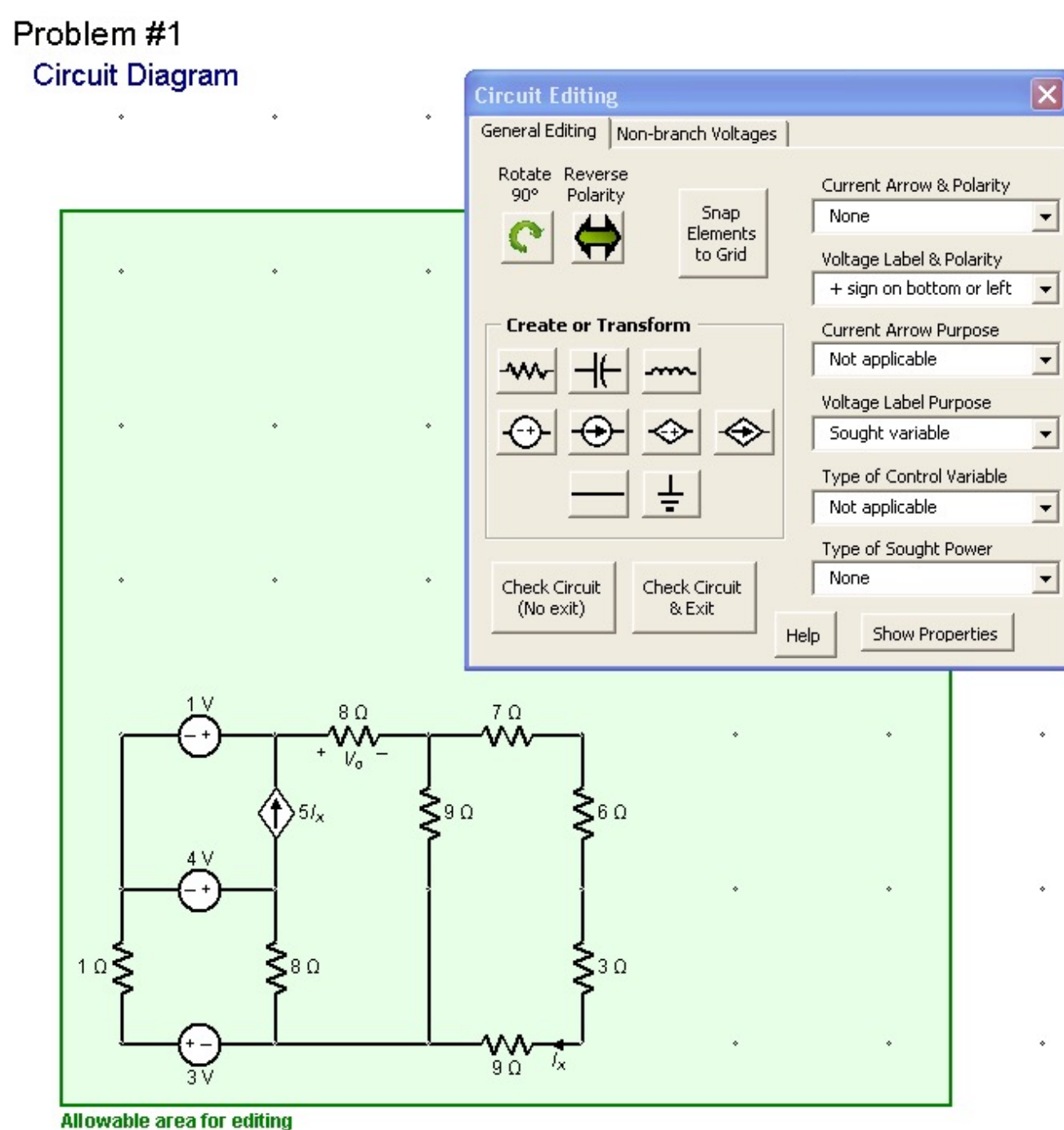
Problem Specification Tab & Advanced Options Dialog Box



Software Modules Under Development

- Problem Generation Module**
 - Generates unlimited supply of circuits similar to textbook problems and examples according to user specifications, randomly varying topology of circuit as well as element values
 - Will be able to generate DC, AC steady state, transient (switched), Laplace analysis, and op-amp circuits
- Solution Generation Module**
 - Goal is to generate fully worked solutions very similar to those found in solution manuals, but in a clearer, more consistent format and free of errors, without requiring human labor
 - Solution techniques will include voltage and current division, combination of elements in series and parallel, nodal and mesh analysis, superposition, source transformation, use of Thévenin & Norton equivalents, and combinations of the above methods.
- Student Input & Validation Modules**
 - Program will accept rich variety of inputs, including numerical inputs in tables, matrices & vectors, equations (in both structured and unstructured formats), re-drawn (graphically edited) circuits (e.g., as steps in a solution), and waveform sketches generated using a graphical drawing interface
 - Above inputs will be checked against computer-generated solutions, giving in-depth feedback to the student
- Problem Generation Interface Module**
 - Will allow instructors to specify numbers and types of problems using a high-level description, including levels of difficulty; can optionally specify more details
- Tutorial Interface Module**
 - Will present tutorial scripts to student, which make use of the other modules
 - Will track performance and provide real-time feedback to instructor as to major points of difficulty being experienced by the class

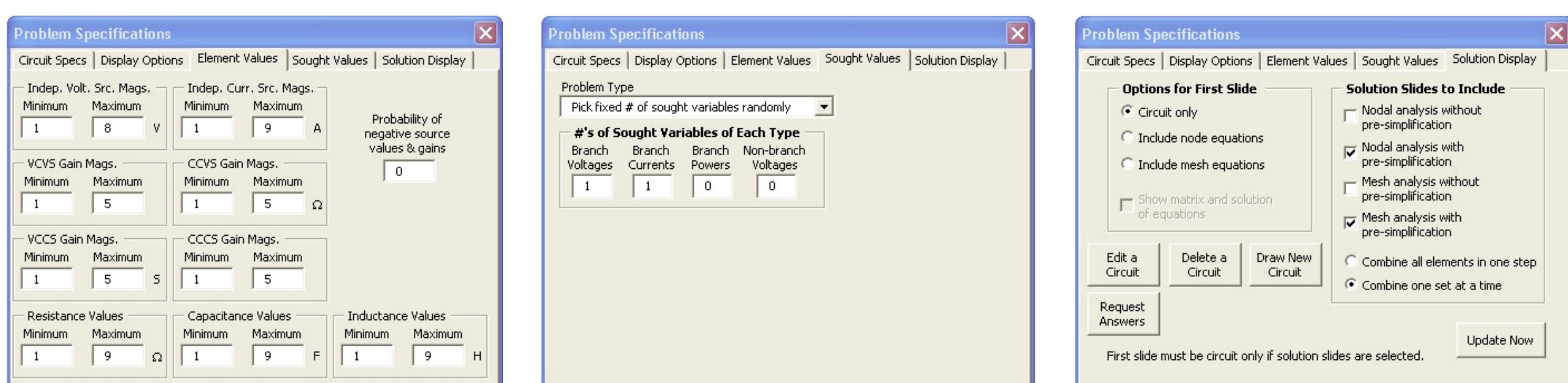
Circuit Editing and Drawing Interface



Pedagogical Features

- Can color code nodes to help identify them
- Can color series & parallel sets red to highlight them
- Can color code currents leaving a node or supernode and voltage drops around a loop

Additional User Interface Tabs (Testing/Demonstration Interface)



Acknowledgments

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Criteria for Acceptable Circuits

- Both node & mesh equations should be uniquely solvable (not singular). Requires that "dead" (inactivated) circuit be both fully connected and "coupled" (can pass from one mesh to any other, including the exterior mesh, by passing over a resistor)²
- We ensure solvable equations (in the absence of dependent sources) by placing all voltages sources & inductors on the twigs of a tree of the network, and all current sources & capacitors on the links.³ (Restrictions are lifted on inductors and capacitors in steady-state AC case.)
- Circuits that are singular due to dependent sources are simply rejected and the process is re-started (occurs rarely)
- Other requirements to be similar to most textbook problems:
 - Circuit should be fully connected
 - Circuit should not be "hinged," i.e., cannot be re-drawn so that two or more portions are connected only by a single wire (excludes shorted elements & "dangling" elements, in particular)
 - Optionally, "redundant" elements that serve no useful purpose in the circuit can be prohibited (such as any element in series with an ideal current source, in parallel with an ideal voltage source, or more general cases such as these)
 - Number of independent voltage sources in series and independent current sources in parallel can be limited to any value ≥ 1
 - Mesheres of shorts are prohibited (reduce number of "true" meshes)
 - Optionally, circuits where all node voltages are determined directly by voltage sources or all mesh currents are determined directly by current sources can be prohibited
 - Control variables for dependent sources must be the voltage or current of a passive element
 - Control variables cannot be derived from an element in series or in parallel with the dependent source they control (except in single node-pair or single loop circuits)
 - Each branch voltage (or those in parallel with it) and branch current (or those in series with it) can be used only once as a control variable

Assessment Strategy (Future Work)

- Assessment will be conducted by Prof. Robert Atkinson at ASU, an expert in evaluating computer-based learning environments
- Formative assessment will include surveys of other instructors concerning preliminary versions of the software modules and instructional sequences, and surveys of students
- Embedded assessment in the tutorial system will be used to assess student usage and progress
- Control sections who do not use our products will be used as a comparison group, assigning them identical but non-interactive exercises as homework
- Surveys and focus groups will be used with faculty and students who use the final version to measure satisfaction, & we will track number of students impacted
- Quantitative data will be analyzed on drop rates, exam & homework scores, and concept inventory pre- and post-tests in both experimental and control sections, carefully controlling for other variables such as major and prior GPA
- Some examinations will be graded using rubrics designed to measure progress towards specific learning objectives

Summary

- Software modules will generate random linear circuit problems similar to those in textbooks, as well as fully worked solutions following methods typically taught in introductory circuit analysis courses
- System will accept student inputs in form of equations, numerical answers, matrices & vectors, re-drawn (graphically edited) circuits, and waveform sketches
- Modules will be incorporated into a tutorial system (scripts currently under development at South Mountain Community College (Prof. T. Frank) in collaboration with ASU
- Eventual goal is open-source distribution and/or commercialization via integration with textbook publisher web site that supports circuits textbooks (e.g., WileyPLUS)
- Additional partners and software users are always being sought!

For Further Information or to Participate in this Project

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